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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/019,189	12/20/2001	Yoshimasa Okabe	8861.417US(P	1363

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EXAMINER	
POPHAM, JEFFREY D	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/019,189	OKABE ET AL.	
	Examiner	Art Unit	
	Jeffrey D. Popham	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23 and 24* is/are allowed.

6)☒ Claim(s) *1-9,13,14,16,17,19-22 and 25* is/are rejected.

7)☒ Claim(s) *10-12,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20011220*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Remarks

Claims 1-25 are pending.

Claim Objections

1. Claims 10, 12, and 21 are objected to because of the following informalities:

   - In Claim 10, lines 17-18, "central processing unit with first scrambling pattern" should apparently read "central processing unit with a first scrambling pattern".
   - In Claim 10, lines 22-23, "descrambled with first scrambling pattern" should apparently read "descrambled with said first scrambling pattern".
   - In Claim 12, line 5, "touched from outside" should apparently read "touched from the outside".
   - In Claim 21, lines 19-20, "the internal circuit of said central processing unit" should apparently read "the internal logic circuit of said central processing unit".

   Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinji (Japanese Patent Application Publication 63-223850).

Regarding Claim 1,

Shinji discloses a production method for an electronic apparatus comprising a board having a separable region, the board being mounted with a CPU, an electronically alterable nonvolatile storage device, and a connector mounted on the region, wherein when the region is separated, data cannot be written to the storage device by directly controlling an internal circuit of the CPU, the production method comprising (Figure 1 and Abstract):

A writing step of writing data to the storage device by connecting an external apparatus to the connector and by directly controlling an internal logic circuit of the CPU (Abstract); and

A separating step of separating the region after the writing step (Abstract).

Regarding Claim 2,

Shinji discloses that the CPU is sealed in such a manner that, when mounted on the board, terminals of the CPU cannot be touched from outside (Figure 1).

Regarding Claim 20,

Shinji discloses an electronic apparatus comprising a board having a separable region, the board being mounted with a CPU, an electrically

alterable nonvolatile storage device, and a connector mounted on the region (Figure 1 and Abstract), wherein:

When the region is not separated yet, data can be written to the storage device by connecting an external apparatus to the connector and directly controlling an internal logic circuit of the CPU (Abstract), and

When the region is separated, data cannot be written to the storage device by controlling the CPU (Abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 5, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinji in view of Shinobu (Japanese Application Publication 64-025354).

Regarding Claim 4,

Shinji discloses a production method for an electronic apparatus comprising a board having a separable region, the board being mounted with a CPU, an electrically alterable nonvolatile storage device, and a connector (Figure 1 and Abstract), the production method comprising:

A writing step of writing data to the storage device by connecting an external apparatus to the connector and by directly controlling an internal logic circuit of the CPU (Abstract); and

A separating step of separating the region after the writing step (Abstract);

But does not disclose a relaying device for connecting at least one terminal of the connector to at least one terminal of the CPU and detection device for detecting whether the region is separated or not.

Shinobu, however, discloses a relaying device for connecting at least one terminal of the connector to at least one terminal of the CPU, and a detection device for detecting whether the region is separated or not, wherein when the region is separated, the relaying device, based on an output signal from the detection device, disconnects at least one connecting line connecting the terminal of the connector to the terminal of the CPU so that data cannot be written to the storage device by directly controlling an internal circuit of the CPU (Figure and Abstract). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the disk device of Shinobu into the access protecting IC card of Shinji in order to prevent incorrectly enciphered data from being written to the IC card.

Regarding Claim 5,

Shinji discloses that all of the components (except for input/output) are sealed in such a manner that, when mounted on the board, the terminals cannot be touched from the outside (Figure 1).

Regarding Claim 21,

Shinji discloses an electronic apparatus comprising a board having a separable region, the board being mounted with a CPU, an electrically alterable nonvolatile storage device, and a connector (Figure 1 and Abstract), wherein:

When the region is not separated yet, data can be written to the storage device by connecting an external apparatus to the connector and directly controlling an internal logic of the CPU (Abstract);

But does not disclose a relaying device for connecting at least one terminal of the connector to at least one terminal of the CPU and a detection device for detecting whether the region is separated or not.

Shinobu, however, discloses a relaying device for connecting at least one terminal of the connector to at least one terminal of the CPU, and a detection device for detecting whether the region is separated or not, wherein when the region is separated, the relaying device, based on an output signal from the detection device, disconnects at least one connecting line connecting the terminal of the connector to the terminal of the CPU so that data cannot be written to the storage device by directly controlling the internal logic of the CPU (Figure and Abstract). It would

have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the disk device of Shinobu into the access protecting IC card of Shinji in order to prevent incorrectly enciphered data from being written to the IC card.

4. Claims 6-9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinji in view of Shinobu, further in view of Ashe (U.S. Patent 6,282,651).

Regarding Claim 6,

Shinji discloses a production method for an electronic apparatus comprising a board having a separable region, the board being mounted with a CPU, an electrically alterable nonvolatile storage device, and a connector (Figure 1 and Abstract), wherein:

When the region is not separated yet, data read out of the storage device can be transferred to the CPU, and by connecting an external apparatus to the connector and directly controlling an internal logic circuit of the CPU, the CPU can be caused to output data to the storage device (Abstract); and

When the region is separated, data read out of the storage device can be transferred to the CPU, but the CPU cannot write data to the storage device (Abstract),

The production method comprising:

A writing step in which by connecting the external apparatus to the connector and directly controlling the internal logic circuit of the CPU, the CPU is caused to output data to the storage device (Abstract); and

A separating step of separating the region after the writing step (Abstract);

But does not disclose a relaying device for connecting at least one terminal of the connector to at least one terminal of the CPU, a detection device for detecting whether the region is separated or not, and a scrambling device capable of scrambling data before writing it to the storage device and descrambling data being read from the storage device.

Shinobu, however, discloses a relaying device for connecting at least one terminal of the connector to at least one terminal of the CPU and a detection device for detecting whether the region is separated or not, and that, when the region is separated, data cannot be written to the storage device (Figure and Abstract). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the disk device of Shinobu into the access protecting IC card of Shinji in order to prevent incorrectly enciphered data from being written to the IC card.

Ashe, however, discloses a scrambling device capable of scrambling data before writing it to the storage device and descrambling data being read from the storage device (Column 2, line 36 to Column 3,

line 61). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the encryption device of Ashe into the access protecting IC of Shinji as modified by Shinobu in order to increase the security of the data stored in memory.

Regarding Claim 22,

Claim 22 is an apparatus claim that is broader than production method claim 6 and is rejected for the same reasons.

Regarding Claim 7,

Shinji discloses that the relaying device, the scrambling device, and other circuits essential to the operation of the electronic apparatus are contained in a single semiconductor device (Abstract).

Regarding Claim 8,

Shinji discloses that all of the components of the apparatus are sealed in such a manner that, when mounted on the board, terminals of the central processing unit and the semiconductor device cannot be touched from outside (Figure 1).

Regarding Claim 9,

Shinji as modified by Shinobu and Ashe discloses the production method of claim 6, in addition, Shinobu discloses that when the region is separated, a line used to transfer all write signals, which include a write strobe signal, from the CPU to the storage device is disconnected (Abstract).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinji in view of Eng (U.S. Patent 6,365,833).

Shinji discloses at least one connecting line connecting between the CPU and the connector and that the connector is formed in the inside (Figure 1 and Abstract), but does not disclose that the board is a multi-layer board of at least four layers.

Eng, however, discloses that the board is a multi-layer board consisting of at least four layers (Column 3, lines 18-31). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the multi-layer circuit board of Eng into the access protecting IC card of Shinji in order to increase security of the information on chip by preventing malicious entities from illegally obtaining information from the chip by disassembling it.

6. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinji in view of Shinobu, further in view of Eng.

Regarding Claim 13,

Shinji as modified by Shinobu discloses the production method of claim 4, in addition, Shinobu discloses a line used to carry a detection signal indicating whether the region is separated or not (Figure and Abstract) and Shinji discloses that the components are formed in an inner layer (Figure 1 and Abstract); but Shinji as modified by Shinobu does not

disclose that the board is a multi-layer board consisting of at least four layers.

Eng, however, discloses that the board is a multi-layer board consisting of at least four layers (Column 3, lines 18-31). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the multi-layer circuit board of Eng into the access protecting IC card of Shinji as modified by Shinobu in order to increase security of the information on chip by preventing malicious entities from illegally obtaining information from the chip by disassembling it.

Regarding Claim 16,

Shinji as modified by Shinobu discloses the production method of claim 4, in addition, Shinobu discloses at least one connecting line connecting between the CPU and the relaying device (Figure and Abstract) and Shinji discloses that the components are formed in an inner layer (Figure 1 and Abstract); but Shinji as modified by Shinobu does not disclose that the board is a multi-layer board consisting of at least four layers.

Eng, however, discloses that the board is a multi-layer board consisting of at least four layers (Column 3, lines 18-31). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the multi-layer circuit board of Eng into the access protecting IC card of Shinji as modified by Shinobu in order to increase

security of the information on chip by preventing malicious entities from illegally obtaining information from the chip by disassembling it.

7. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinji in view of Shinobu and Ashe, further in view of Eng.

Regarding Claim 14,

Shinji as modified by Shinobu and Ashe discloses the production method of claim 6, in addition, Shinobu discloses a line used to carry a detection signal indicating whether the region is separated or not (Figure and Abstract) and Shinji discloses that the components are formed in an inner layer (Figure 1 and Abstract); but Shinji as modified by Shinobu and Ashe does not disclose that the board is a multi-layer board consisting of at least four layers.

Eng, however, discloses that the board is a multi-layer board consisting of at least four layers (Column 3, lines 18-31). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the multi-layer circuit board of Eng into the access protecting IC card of Shinji as modified by Shinobu and Ashe in order to increase security of the information on chip by preventing malicious entities from illegally obtaining information from the chip by disassembling it.

Regarding Claim 17,

Shinji as modified by Shinobu and Ashe discloses the production method of claim 4, in addition, Shinobu discloses at least one connecting line connecting between the CPU and the relaying device (Figure and Abstract) and Shinji discloses that the components are formed in an inner layer (Figure 1 and Abstract); but Shinji as modified by Shinobu and Ashe does not disclose that the board is a multi-layer board consisting of at least four layers.

Eng, however, discloses that the board is a multi-layer board consisting of at least four layers (Column 3, lines 18-31). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the multi-layer circuit board of Eng into the access protecting IC card of Shinji as modified by Shinobu and Ashe in order to increase security of the information on chip by preventing malicious entities from illegally obtaining information from the chip by disassembling it.

8. Claims 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinji in view of Shandle (Shandle "The Silent Advantage", *Electronics*, 12/1991, pp. 30 and 32, obtained from http://proquest.umi.com/pqdweb?did=1628860&sid=2&Fmt=2&clientId=19649&RQT=309&VName=PQD).

Regarding Claim 19,

Shinji does not disclose that the CPU is an IEEE 1149 compliant device.

Shandle, however, discloses that the CPU is an IEEE 1149 compliant device (Pages 30 and 32). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the boundary-scan testing of Shandle into the access protecting IC card of Shinji in order to allow the IC to be easily tested and debugged via a standard interface.

Regarding Claim 25,

Shinji does not disclose that the CPU is an IEEE 1149 compliant device.

Shandle, however, discloses that the CPU is an IEEE 1149 compliant device (Pages 30 and 32). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the boundary-scan testing of Shandle into the access protecting IC card of Shinji in order to allow the IC to be easily tested and debugged via a standard interface.

Allowable Subject Matter

9. Claims 10-12, 15, 18, 23, and 24 are allowable if the objections stated above in regards to claims 10 and 12 are overcome. The following is a statement of reasons for the indication of allowable subject matter:

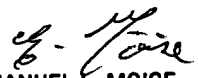
The closest prior art discloses that which is in independent claims 1, 4, 6, 20, 21, and 22, but independent claims 10, 23, and 24 include the additional limitation that the encryption algorithm is changed at the time of separation. The mere use of multiple encryption algorithms within the system would not be deemed allowable, but the fact that the encryption algorithm is changed, in this particular apparatus, at the time the separable portion of the board is separated from the rest of the board, makes the claims allowable over the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey D. Popham whose telephone number is (571)-272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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